LVDT/RVDT - A linear variable differential transformer (LVDT) is a type of electrical transformer/transducer used for measuring linear displacement (position). A counterpart to this device used for measuring rotary displacement is called a rotary variable differential transformer (RVDT). The RVDT is like an LVDT in that it measures a positional displacement, however, the displacement, which is still a linear proportional function, is based on rotary instead of linear positional movement. Both deliver signals proportional to the linear displacement of the moveable core.

Simulation

Module	Description
DLA	2 Ch. Output (2-28 RMS), Output 1.5VA at 28Vrms, Frequency 47 – 1,000 Hz
DLB	2 Ch. Output (2-28 RMS), Output 1.5VA at 28Vrms, Frequency 1,000 – 5,000 Hz
DLC	2 Ch. Output (2-28 RMS), Output 1.5VA at 28Vrms, Frequency 5,000 – 10,000 Hz
DLD	2 Ch. Output (2-28 RMS), Output 1.5VA at 28Vrms, Frequency 10,000 – 20,000 Hz
DLE	2 Ch. Output (28 - 90 RMS), Output 2.2 VA at 90Vrms, Frequency 47 – 1000 Hz
DLJ	3 Ch. Output (2-28 RMS), Output .5VA at 28Vrms, Frequency 47 – 1,000 Hz
DLK	3 Ch. Output (2-28 RMS), Output .5VA at 28Vrms, Frequency 1,000 – 5,000 Hz
DLL	3 Ch. Output (2-28 RMS), Output .5VA at 28Vrms, Frequency 5,000 – 10,000 Hz
DLM	3 Ch. Output (2-28 RMS), Output .5VA at 28Vrms, Frequency 10,000 – 20,000 Hz
DLN	3 Ch. Output (28 – 90 RMS), Output .5VA at 90Vrms, Frequency 47 – 1000 Hz

Key Features

NAI offers five smart function modules that convert these signals to a digital output corresponding to position in a variety of operating parameters. An LVDT/RVDT simulator is used to convert digital positional commands to corresponding AC signals.

Built-In Test (BIT)/Diagnostic Capability
The board supports three types of built-in tests: Power-On, Continuous Background and Initiated. The results of these tests are logically ORed together and stored in the BIT Dynamic Status and BIT Latched Status registers.

Power-On Self-Test (POST) / Power-on BIT (PBIT) / Start-up BIT(SBIT)
This board features a power-on self-test that will do an accuracy check of each channel and report the results in the BIT Status register when complete. After power-on, the Power-on BIT Complete register should be checked to ensure that POST/PBIT/SBIT test is complete before reading the BIT Latched Status.

Continuous Background Built-In Test
The background Built-In-Test or Continuous BIT (CBIT) (“D2”) runs in the background where each channel is checked to a test accuracy of 0.2% FS. The testing is totally transparent to the user, requires no external programming, and has no effect on the operation of the module or card. The technique used by the continuous background BIT (CBIT) test consists of an “add-2, subtract-1” counting scheme. The BIT counter is incremented by 2 when a BIT-fault is detected and decremented by 1 when there is no BIT fault detected and the BIT counter is greater than 0. When the BIT counter exceeds the (programmed) Background BIT Threshold value, the specific channel’s fault bit in the BIT status register will be set. Note, the interval at which BIT is performed is dependent and differs between module types. Rather than specifying the BIT Threshold as a “count”, the BIT Threshold is specified as a time in milliseconds. The module will convert the time specified to the BIT Threshold “count” based on the BIT interval for that module. The “add-2, subtract-1” counting scheme effectively filters momentary or intermittent anomalies by allowing them to “come and go“ before a

BIT fault status or indication is flagged (e.g. BIT faults would register when sustained; i.e. at a ten second interval, not a 10-millisecond interval). This prevents spurious faults from registering valid such as those caused by EMI and/or dirty power causing false BIT faults. Putting more “weight” on errors (“add-2”) and less “weight” on subsequent passing results (subtract-1) will result in a BIT failure indication even if a channel “oscillates” between a pass and fail state.

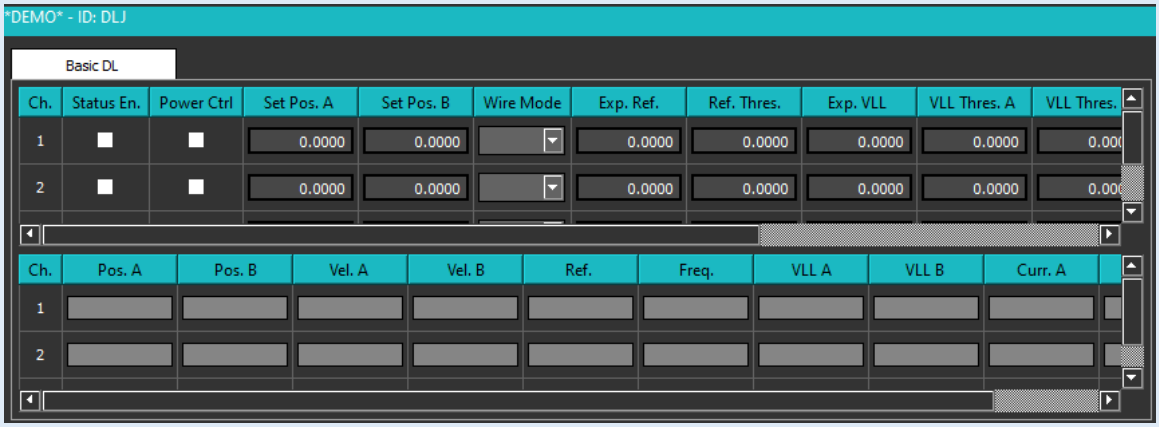
Initiate Built-In Test

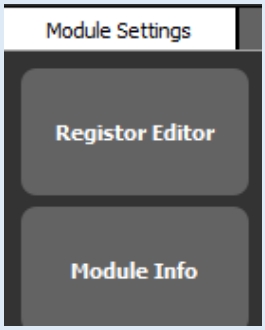
The DLx module supports an off-line Initiated Built-In Test (IBIT) (“D3”). IBIT test starts an initiated BIT test that utilizes an internal stimulus to generate and test the full-scale positional range to a default test accuracy of 0.1% full scale range. IBIT test cycle is completed within 30 seconds and the result can be read from the BIT status registers when IBIT bit changes from 1 to 0.

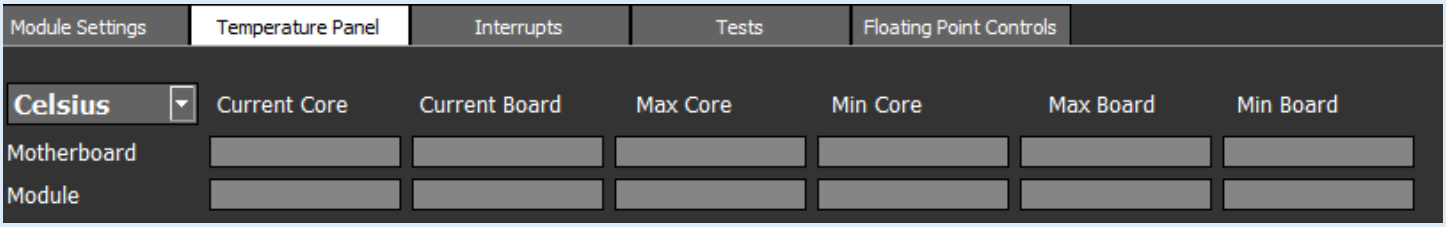
New Embedded Soft Panel

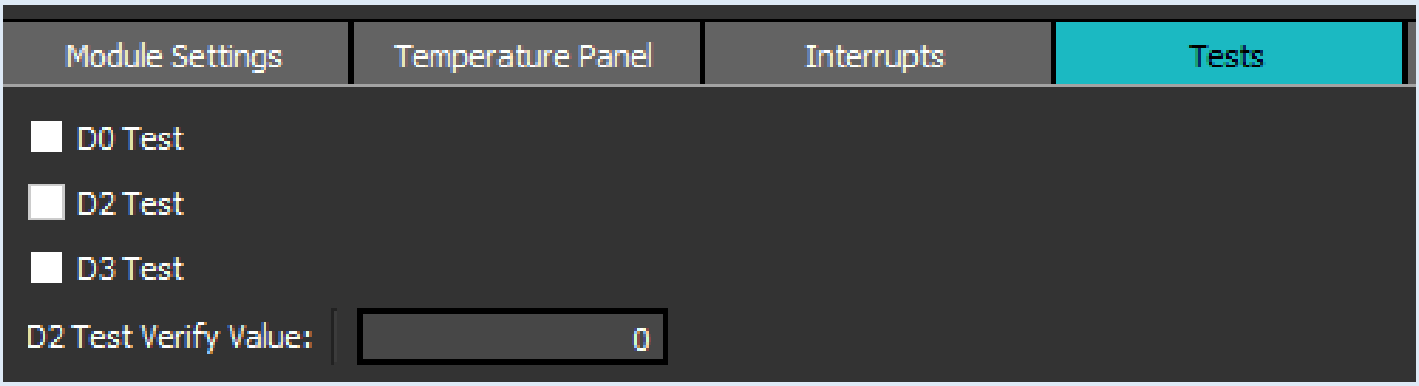
North Atlantic Industries offers the newest cross platform (Windows and Linux) GUI for our Gen 5 products that allows a user to quickly interact with our broad range of modular, I/O cards and rugged embedded computing products. Embedded Soft Panel 2 (ESP 2) is coherent and easy to use with a clean, fleshed out UI with features such as drag and drop dock able windows, a dark and light theme, and multi-language support. Multiple ways to open a board are offered, including saving board opening settings for future use. Interacting with and collecting information on hardware is simple to do with the register editor for reading and writing specific addresses, and the API logger which logs all API library calls including their return status and parameters. ESP 2 has many new features and provides an organized and effortless interface for NAI’s next generation products. Available for CentOS 7.4 and 8.2 and Windows 10 x64

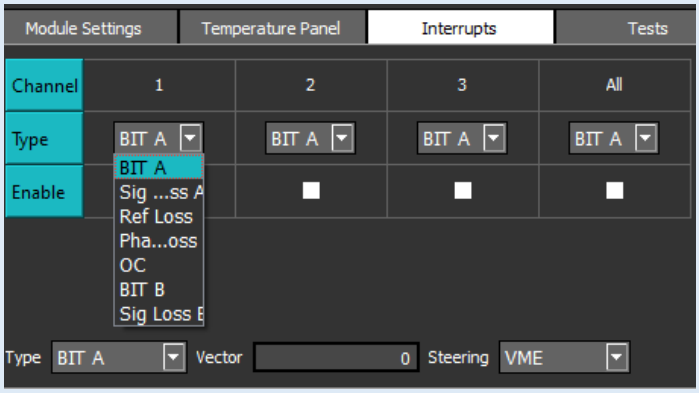
LVDT/RVDT Simulation Example - Module DLJ Demo Mode Screen Shots











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